

What is claimed is:

1. 1. An addition circuit for producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:
 2. a 4:2 compression adder for receiving each of the operand fields of the four redundant binary numbers, and producing a first sum field and a first carry field therefrom;
 3. a 4:3 compression adder for receiving each of the sparse carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom;
 4. a 3:2 compression adder for receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;
 5. wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.
1. 2. An addition circuit according to claim 1, wherein the 4:2 compression adder includes a cascade of a first full adder and a second full adder.
1. 3. An addition circuit according to claim 1, wherein the 4:3 compression adder includes a binary summer for receiving four input bits of equal weight, and producing a three bit binary output word representative of the sum of the four input bits.
1. 4. An addition circuit according to claim 1, wherein the 3:2 compression adder includes a full adder.
1. 5. An addition circuit according to claim 1, wherein the 4:3 compression adder distributes bits within the second sum field so as to correspond to the significance of the sparse carry-save field.

1 6. An addition circuit according to claim 1, wherein each of the four redundant binary
2 numbers is in radix-16 format, so as to include a sparse carry-save bit for every four operand bits.

1 7. An addition circuit for producing a sum of four redundant binary numbers, wherein each
2 number includes an operand field and a sparse carry-save field, comprising:

3 means for receiving each of the operand fields of the four redundant binary numbers, and
4 producing a first sum field and a first carry field therefrom;

5 means for receiving each of the sparse carry-save fields of the four redundant binary
6 numbers, and producing a second sum field therefrom;

7 means for receiving the first sum field, the first carry field and the second sum field, and
8 producing a third sum field and a second carry field therefrom;

9 wherein the third sum field and the second carry field are the sum of the four redundant
10 binary numbers.

1 8. An addition circuit according to claim 7, wherein the means for receiving each of the
2 operand fields includes a cascade of a first full adder and a second full adder.

1 9. An addition circuit according to claim 7, wherein the means for receiving each of the
2 carry-save fields includes a binary summer for receiving four input bits of equal weight, and
3 producing a three bit binary output word representative of the sum of the four input bits.

1 10. An addition circuit according to claim 7, wherein the means for receiving the first sum
2 field, the first carry field and the second sum field includes a full adder.

1 11. An addition circuit according to claim 7, wherein the means for receiving each of the
2 carry-save fields distributes the second sum field so as to correspond to the significance of the
3 sparse carry-save field.

1 12. An addition circuit according to claim 7, wherein each of the four redundant binary
2 numbers is in radix-16 format, so as to include a sparse carry-save bit for every four operand bits.

1 13. A method of producing a sum of four redundant binary numbers, wherein each number
2 includes an operand field and a sparse carry-save field, comprising:

3 receiving each of the operand fields of the four redundant binary numbers, and producing
4 a first sum field and a first carry field therefrom;

5 receiving each of the carry-save fields of the four redundant binary numbers, and
6 producing a second sum field therefrom;

7 receiving the first sum field, the first carry field and the second sum field, and producing
8 a third sum field and a second carry field therefrom;

9 wherein the third sum field and the second carry field are the sum of the four redundant
10 binary numbers.

1 14. A method according to claim 13, further including using a 4:2 compression adder to
2 produce the first sum field and the first carry field.

1 15. A method according to claim 13, further including using a 4:3 compression adder to
2 produce the second sum field.

1 16. A method according to claim 13, further including using a 3:2 compression adder to
2 produce the third sum field and the second carry field.

1 17. A method according to claim 13, further including distributing bits within the second sum
2 field so as to correspond to the significance of bits within the sparse carry-save field.

1 18. An addition circuit for producing a sum of four redundant binary numbers, wherein each
2 number includes an operand field and a sparse carry-save field, comprising:
3 a 4:2 compression adder, including a cascade of a first full adder and a second full adder,
4 for receiving each of the operand fields of the four redundant binary numbers, and producing a
5 first sum field and a first carry field therefrom;
6 a 4:3 compression adder, including a binary summer for receiving four input bits of equal
7 weight and producing a three bit binary output word representative of the sum of the four input
8 bits, for receiving each of the carry-save fields of the four redundant binary numbers, and
9 producing a second sum field therefrom;
10 a 3:2 compression adder, including a full adder, for receiving the first sum field, the first
11 carry field and the second sum field, and producing a third sum field and a second carry field
12 therefrom;
13 wherein the third sum field and the second carry field are the sum of the four redundant
14 binary numbers.

1 19. A method of producing a sum of four redundant binary numbers, wherein each number
2 includes an operand field and a sparse carry-save field, comprising:
3 receiving each of the operand fields of the four redundant binary numbers, and producing,
4 via a 4:2 compression adder, a first sum field and a first carry field therefrom;
5 receiving each of the carry-save fields of the four redundant binary numbers, and
6 producing, via a 4:3 compression adder, a second sum field therefrom;
7 receiving the first sum field, the first carry field and the second sum field, and producing,
8 via a 3:2 compression adder a third sum field and a second carry field therefrom;
9 wherein the third sum field and the second carry field are the sum of the four redundant
10 binary numbers.

1 20. A method of producing a sum of at least two redundant binary numbers, wherein each
2 number includes an operand field and a sparse carry-save field, comprising:
3 receiving each of the operand fields of the at least two redundant binary numbers, and
4 producing a first sum field and a first carry field therefrom;
5 receiving each of the sparse carry-save fields of the four redundant binary numbers, and
6 producing a second sum field therefrom, wherein a distribution of bits within the second sum
7 field corresponds to a sparse distribution within the sparse carry-save fields;
8 receiving the first sum field, the first carry field and the second sum field, and producing
9 a third sum field and a second carry field therefrom;
10 wherein the third sum field and the second carry field are the sum of the four redundant
11 binary numbers.